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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,875	06/11/2001	Abu K. Eghan	X-901 US	4969

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,875	EGHAN ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-15* is/are allowed.

6)☒ Claim(s) *1-7 and 9-12* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Bhattacharyya et al. (U.S. Patent 5,608,261) [in view of a "secondary reference" to Wakabayashi et al. (U.S. Patent 4,598,307) for teaching inherent and notoriously well known properties of a "*by-pass* capacitor"].

Bhattacharyya et al. disclose an "integrated circuit package substrate" (10) comprising: "a recessed central region" (i.e. that is stepped, has chip 20, and bonding shelves 13 and 15) having a "plurality of contacts for providing electrical contact to an integrated circuit device" (i.e. inherent bonding wire contacts on bonding shelves 13 and 15 that electrically connect to chip 20); and "a raised peripheral area *including* capacitors 22 and 23" that are *inherently* "connected to contacts within the recessed central region".

Bhattacharyya et al. does not use the word "by-pass" to describe the intended effect of the implementation of (by-pass) capacitors 22 and 23 in their package substrate. However, capacitors 22 and 23 in Bhattacharyya et al. are *inherently* by-pass capacitors in view of the teaching of Wakabayashi et al. (U.S. Patent 4,598,307):

> In order to protect ICs from noise it is necessary to mount a bypass capacitor as close as possible to the IC die or chip...In order to reduce the problem [of noise], a capacitor (i.e. a "by-pass capacitor") is provided between the power source and ground [abstract + column 1, lines 10-20].

Capacitors 22 and 23 in Bhattacharyya et al. are inherently "by-pass capacitors" because, like applicant's "by-pass capacitor(s)", Bhattacharyya et al.'s capacitors are "connected between power and ground" and provide:

> ...large capacitance noise filtering while remaining compatible with thermal dissipation techniques [col. 2, lines 20-24].

3. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Eda et al. (U.S. Patent 5,387,888).

Eda et al. disclose an "integrated circuit package substrate" (visible in the cover figure as a substrate supporting transistor "integrated circuit device" 209) comprising: "a recessed central region" (visible as a recessed region receiving transistor integrated circuit device 209) having a "plurality of contacts for providing electrical contact to an integrated circuit device" (i.e. inherent contacts of conductive 201 that electrically connect to transistor integrated circuit device 209); and "a raised peripheral area *including* by-pass capacitors [e.g. col. 3, line 58].

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Crane et al. (U.S. Patent 5,892,280).

Regarding claim 1, Crane et al. teach "a packaged integrated circuit device" [e.g. Figs. 3 and 4] comprising a substrate 14 having a recessed central region surrounded by raised perimeter being formed integrally" (i.e. integrally per col. 10, line 58 and the recess seen as receiving "integrated circuit device comprising chip 11 on carrier 12" in Figs. 3 and 4), the recess having plurality of contacts 13 within the central region for inherently "providing electrical connection from conductors external to the substrate" to "an integrated circuit device" (e.g. 11); and "an integrated circuit device formed with contacts 13 on a top surface (i.e. inherently on the "top surface" of a wafer), flipped, and placed in the central region so "the contacts" of "the recessed central region of the substrate" inherently "meet the contacts of the integrated circuit device" (i.e. "device" comprising chip-on-carrier 11/12).

Regarding claim 5, contacts 13 are "preferably solder balls."

5. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Tosaki et al. (U.S. Patent 6,272,020).

Regarding claim 1, Tosaki et al. disclose a "packaged integrated circuit device" wherein an integrated circuit "capacitor device 4" is inherently "packaged" (with chip 2 on substrate 3) comprising: a substrate 3 having raised periphery with central recessed region wherein substrate 3 is formed integrally (by firing *ceramic* green sheets) with all other limitations of claim 1 anticipated when properly considering "capacitor chip device 4" as an "integrated circuit device" since it is reasonable "integrated" with chip(s) and substrate(s), it is inherently a "circuit element", and it is named by Tosaki et al. as a "device."

Regarding claim 2, the solder balls 8A and 8C correspond to the claimed "balls on an external surface."

Regarding claim 3, the substrate 3 is "primarily ceramic" [col. 5, lines 45-48].

Regarding claim 9, the "raised perimeter" inherently includes "power" and "ground" because all operational semiconductor chips inherently have "power" and "ground" and, as seen in the cover figure, all circuitry leading to the external world from chip 2 passes through the "raised periphery" delineated on the right by "3B".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 an 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane et al. (U.S. 5,892,280) as applied to claim 1 above, and further in view of U.S. Patent 5,723,369.

Regarding claims 6 and 7, Crane et al. does not teach a heat spreader connected to the device with "thermal grease", and only explicitly teaches thermally conductive epoxy 20 (visible between cap 21 and device 11/12 as seen in Fig. 4).

The '369 patent teaches a generalized equivalence of "thermal grease" with "thermal conductive epoxy":

> To aid in conducting heat away from the integrated circuit, heat conductive media such as thermal conductive epoxy or thermal grease is placed in the areas between the integrated circuit and the package.... [Brief Summary Text (6)]

Thus, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to substitute "thermal grease" for conductive epoxy in the depicted device in Fig. 4 of Crane et al.. One of ordinary skill in the art would have been motivated by a desire "to aid in conducting heat away from the integrated circuit" as is taught by the '369 patent.

Regarding claim 7, the heat conduction cap 21 (i.e. inherently a "heat spreader") "further contacts the raised perimeter" and even wraps around the raised perimeter, which constitutes an even further form of "further contact."

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tosaki et al. (U.S. 6,272,020) as applied to claim 3 above, and further in view of Fasano et al. (U.S. Patent 6,436,332).

Tosaki et al. does not teach "glass" in their ceramic substrate 3.

Fasano et al. teach a glass-ceramic having a low CTE and low loss tangent [abstract].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have used glass-ceramic as the ceramic in Tosaki et al. for their ceramic substrate 3. One of ordinary skill in the art would have been motivated by a desire to have a substrate having a low CTE matched to the chip (as can be done at the direction of Fasano et al.), and low loss tangent, to reduce parasitic coupling in their interconnecting ceramic substrate 3 [see MPEP 2144 for properness of motivation].

9. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya et al. (U.S. 5,608,261) as applied to claim 10 above, and further in view of Metzler (U.S. Patent 6,368,514).

Bhattacharyya et al. does not teach a "plurality of plates" in by-pass capacitors 22 and 23 "included" (connected into) the raised perimeter and inherently connected between power and ground.

Fromont teaches "batch film capacitors" that are suitable for connecting into the raised periphery as capacitors 22 and 23 taught by Bhattcharyya et al. As seen in Fig. 13B of Fromont, these particular type of capacitors have increased capacitance by the plurality of plates connected to each of the two capacitor terminals.

It would have been obvious to use a capacitor of the type taught by Metzler as discrete capacitor 22 and/or 23 in Bhattacharyya et al.. This use of Metzler's capacitors would inherently meet the limitations of "sandwich construction", "plurality of ground plates", and "plurality of power plates" with "insulating material disposed between adjacent plates." One of ordinary skill in the art would have been motivated to use a capacitor having such a construction because of the greater capacitance desired for a by-pass capacitor provided in a small space as disclosed by Metzler [col. 1, first two paragraphs of Background of Invention].

Response to Arguments

10. Applicant's arguments with respect to claims 1-7 and 9-12 have been considered but are moot in view of the new grounds of rejection.

Allowable Subject Matter

11. Claims 13-15 are allowed.

12. Claim 8 is objected to as being dependent upon a rejected dependent claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The reasons for the indication of allowable subject matter are evident from item 7 of paper 8, and are not repeated here for the sake of brevity.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fromont (U.S. Patent 5,831,825) is cited for teaching an integral substrate with recessed region receiving BGA package 11 "flipped" and contacting contacts in a central region that are electrically connected to pins 17 which are functional equivalents of solder balls, with certain applications for balls more appropriate than pin terminals [col. 1, lines 41-46].

15. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

EVAN PERT

ETP
January 11, 2003